on the high-k dielectric material layer or a silicon oxide layer and a polysilicon layer disposed on the silicon oxide layer. The gate stack structure is configured as a grating structure or as one box of a box-in-box structure. The contact layer may be configured as an inner box of the box-in-box structure. In certain embodiments, the dopant in the semiconductor substrate includes one or more of boron containing compounds, such as boron fluoride (BF_2), arsenic (and/or phosphorus), indium, nitrogen, and carbon. The semiconductor substrate in the overlay region includes silicon and may have a refractive index of about 3 or less.

FIG. **1** is a flowchart of a method **100** for making a semiconductor device according to one embodiment. The semiconductor device includes a metal gate stack and an overlay mark constructed according to various aspects of the present disclosure. FIGS. **2** through **10** are sectional views of a semiconductor structure **200** at various fabrication stages and constructed according to various embodiments. The semiconductor structure **200** and the method **100** of making the same are collectively described with reference to FIGS. **1** through **10**.

Referring to FIGS. **1** and **2**, the method **100** begins at step **102** by providing a semiconductor substrate. The semiconductor substrate includes silicon. Alternatively, the semiconductor substrate includes germanium, silicon germanium or other proper semiconductor materials. The semiconductor substrate also includes various isolation features, such as shallow trench isolation (STI) features formed in the semiconductor substrate to separate various devices. The semiconductor substrate includes an overlay region **212** for an overlay mark and a device region **214** for one or more field-effect transistors (FETs) and/or other devices. Various STI features **216** are formed in the semiconductor substrate **210** in the device region **214**. The formation of the STI features **216** includes etching a trench in a substrate and filling the trench by one or more insulator materials, such as silicon oxide, silicon nitride, or silicon oxynitride. The filled trench may have a multi-layer structure such as a thermal oxide liner layer with silicon nitride filling the trench. In one embodiment, the STI feature **216** is created using a process sequence such as: growing a pad oxide, forming a low pressure chemical vapor deposition (LPCVD) nitride layer, patterning an STI opening using photoresist and masking, etching a trench in the substrate, optionally growing a thermal oxide trench liner to improve the trench interface, filling the trench with CVD oxide, using chemical mechanical planarization (CMP) to etch back, and using nitride stripping to leave the STI features. The semiconductor substrate **210** also includes various n-wells and p-wells formed in various active regions.

Still referring to FIGS. **1** and **2**, the method **100** proceeds to step **104** by performing a first ion implantation to introduce doping species in the semiconductor substrate **210** in the device region **214** and semiconductor substrate **211** in the overlay region **212**. The first ion implantation **218** includes one or more ion implantations implemented before the formation of gate stacks to form various doped features **219**. In one embodiment, the first ion implantation **218** includes a well ion implantation to form a well, such as an n-type well (n-well) or a p-type well (p-well), an ion implantation to adjust threshold voltage, an anti-punch through (APT) ion implantation, or combinations thereof. An ion implantation process **218** is applied to the device region **214** and overlay region **212** such that doping species form the respective doped feature **219** in the device region, and the entire substrate **210** in the overlay region **212** is doped.

In one example, when a p-type dopant is introduced to the semiconductor substrate to form one or more p-wells, an implant mask layer is patterned to cover a portion of the device region for an n-well, then a p-type dopant is introduced to the semiconductor substrate **210** by an ion implantation to form one or more p-wells in the device region **214**. The implant mask layer may be formed using a photolithography process including photoresist coating, soft baking, exposing, post-exposure baking (PEB), developing, and hard baking. The implant mask layer is removed thereafter using a suitable process, such as wet stripping or plasma ashing. Alternatively, a patterned photoresist layer may be used to pattern a hard mask layer to be used as an implant mask. According to various embodiments, the semiconductor portion **211** in the overlay region receives all or most of the dopants implanted in the device region while various portions of the device region are covered during the implantation process to form various features. Thus, the semiconductor portion **211** in the overlay region **212** receives a higher dopant dosage than the semiconductor portion **210** in the device region **214**.

Referring to FIGS. **1**, **3** and **4**, the method **100** proceeds to step **106** by forming gate stacks in the device region **214** and the overlay region **212**. In one embodiment, various gate material layers are formed on the semiconductor substrate **210** and **211** as illustrated in FIG. **3**. The gate material layers include a dielectric material layer **220** and a silicon layer **222**, such as polycrystalline silicon (polysilicon). In the present embodiment, the silicon layer **222** may be non-doped and the dielectric material layer **220** includes a high-k dielectric material layer. The silicon layer **222** alternatively or additionally may include amorphous silicon. The high-k dielectric material layer **220** includes a dielectric material having the dielectric constant higher than that of thermal silicon oxide, which is about 3.9. In one example, the high-k dielectric layer **220** includes hafnium oxide (HfO). In various other examples, the high-k dielectric layer **220** includes metal oxide, metal nitride, or combinations thereof. In one example, the high-k dielectric layer **220** has a thickness ranging between about 10 angstrom and about 100 angstrom.

In various embodiments, the gate material layers include multi-layer dielectric materials, such as an interfacial layer (e.g., silicon oxide) and a high-k dielectric material layer disposed on the interfacial layer. In another embodiment, a hard mask layer **224**, such as silicon nitride (SiN) or silicon oxide (SiO_2), is further formed on the gate material layers for gate patterning. In various embodiments, the interfacial layer may be formed by chemical oxide technique, thermal oxide procedure, atomic layer deposition (ALD) or chemical vapor deposition (CVD). The high-k dielectric material layer may be formed by CVD, ALD, plasma enhanced CVD (PE CVD), or plasma enhanced ALD (PEALD). The non-doped amorphous silicon or polysilicon layer **222** can be formed using CVD with precursor silane (SiH_4) or other silicon based precursor. The deposition of the non-doped amorphous silicon layer **222** can be performed at a raised temperature. The hard mask layer (SiN or SiO_2) can be formed by CVD or other suitable technique.

The gate material layers are patterned to form one or more gate stacks **226** and **228** in the overlay region **212**, and one or more gate stacks (or dummy gates) **229** in the device region **214**, as illustrated in FIG. **4**. The patterning of the gate material layers can be achieved by a lithography process and/or an etch process. For example, a patterned photoresist layer is formed on the hard mask layer **224** defining various gate regions, using a photolithography